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NOVEL DESIGN FOR BCD ADDER WITH MINIMIZED DELAY

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ABSTRACT— In VLSI design of system architecture configuration, the speed is purely determined by the delay of the design. In the delay of the design, it is mainly depending on the routing i.e. path delay. Nowadays in the design, the path or routing delay dominates more towards the design delay when compare to the earlier days where gate delay dominates more towards the design delay. So, it is essential to concentrate more towards routing delay of the design to achieve the optimum speed of the architecture.

In this work, by studying different architectures of BCD adder which is being constructed with different sub-modules which contributes towards the delay estimation, which are realized and implemented on the FPGA.

BCD Adder is designed using reversible gates to reduce delay. A new design of reversible BCD adder having C0 as input carry with no ancilla input bits gives less quantum cost and logic depth. The reversible logic gates find its application like low power CMOS, quantum computing, nano technology and optical computing because of its zero power dissipation. It is done by reducing the number of gates and garbage outputs.

KEYWORDS—BCD Adder, Architecture, Macro, VLSI, routing delay, ancilla input bits, reversible logic gates.

I. INTRODUCTION

For any system design, the arithmetic units are much important to make it as a successful design. In arithmetic unit adders took more contribution to play a vital role since subtraction and multiplication are computed only by means of addition. So, if the speed is achieved by minimizing the delay, in the delay of the architecture of adder and multiplier surely it leads to a better performance in the speed of the design of the high speed system. So, various BCD adder architectures are realized, implemented and their delay is compared.

In modern VLSI system due to rapid switching of internal signals, power dissipation is high. The amount of heat energy is generated in irreversible logic, the computation is easy. Reversible gates do not lose information during logic computation which virtually dissipates zero heat. Adders are fundamental building blocks in

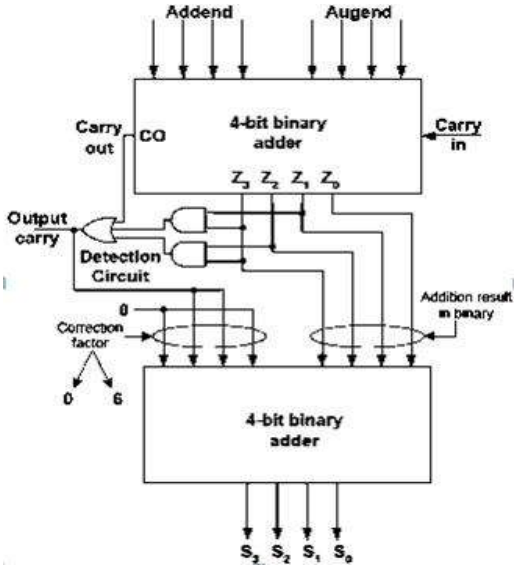
many computational units. It is an easy conversion to digital digits for printing and display faster calculations. One of the major problems with reversible logic is fan out and feedback cannot be used. According to Moore's law, the number of transistors will double in every 18 months.

Today the most important feature in BCD adder is to conserve energy. Binary computing is used in hardware design because of ease in building hardware when compared with decimal computing. This binary computing is not suited for financial and commercial because it cannot tolerate errors. In classical computing usage of digital data using logical operations. In this a single bit of information is erased after every logical operation. Improvement in technology leads to compact size and increase in execution speed. High level of integration and the use of new fabrication process have reduced in the Genetic Algorithms used to synthesize and optimize logic circuit. At present irreversible technologies can reduce the life of the circuit and also dissipate more heat. But in reversible logic operations it does not lose any information and dissipate very less heat.

This paper is organized as follows. Section I says about the Introduction. Section II deals about BCD adder, Section III deals with Literature Survey ,Section IV deals with proposed Architecture, Section V deals with experimental results obtained, while Section VI deals with Conclusion and Discussion.

II. BCD ADDER

The BCD code is a code that combines the features of decimal and binary base number system. In BCD number system a group of binary bit is used to represent each of 10 decimal digits.



BCD numbers are used to transfer the decimal information into a Computer, Packet calculators, electronic counters, digital voltmeters and digital clocks are the applications of BCD numbers. BCD code referred to as 8421 code. Instead of using all combinations (0-15) of only code use (0-9)combinations. 1001 is the largest number in BCD number system. Other numbers 1010,1011,1100,1101,110 and 1111 are not used because these are all considered as forbidden.1001 is the largest 4-bit group in the BCD code. BCD adder is a 4-bit binary adder that is capable of adding two fur bit words having a BCD.

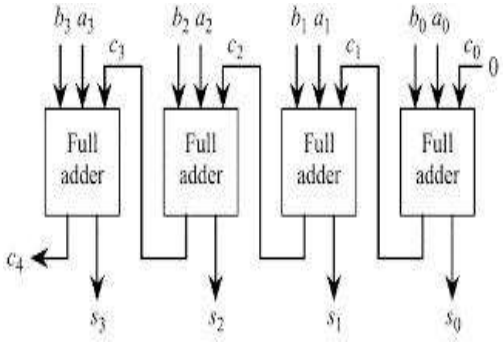


Fig.1 Ripple carry adder

Fig.2 Table for BCD addition.

Binary Sum K	Z8	Z4	Z2	Z1	BCD Sum C	S8	S4	S2	S1	Decimal
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	2
0	0	0	1	1	0	0	0	1	1	3
0	0	1	0	0	0	0	1	0	0	4
0	0	1	0	1	0	0	1	0	1	5
0	0	1	1	0	0	0	1	1	0	6
0	0	1	1	1	0	0	1	1	1	7
0	1	0	0	0	0	1	0	0	0	8
0	1	0	0	1	0	1	0	0	1	9
0	1	0	1	0	1	0	0	0	0	10
0	1	0	1	1	1	0	0	0	1	11
0	1	1	0	0	1	0	0	1	0	12
0	1	1	0	1	1	0	0	1	1	13
0	1	1	1	0	1	0	1	0	0	14
0	1	1	1	1	1	0	1	0	1	15
1	0	0	0	0	1	0	1	1	0	16
1	0	0	0	1	1	0	1	1	1	17
1	0	0	1	0	1	1	0	0	0	18
1	0	0	1	1	1	1	0	0	1	19

Example1: Augent 0110(6)
Addent 0101(5)
Sum 1011(11) (Invalid BCD Number)
Add 0110(6)
BCD 10001(11) (Valid BCD Number)
Answer 0001 0001(11)

Example2: Augent 0011(3)
Addent 0110(6)
Sum 1001(9) (Valid BCD Number)
Add 0000(0)
BCD 1001(9) (Valid BCD Number)
Answer 0000 1001(9)

Reversible logic is used in computing applications and by reducing size and hence portability of the devices are increase. The result of the addition is in a BCD format four bit output word representing the decimal sum of the Addend & Augent and a carry that is generated. If this sum exceeds a decimal value of nine, decimal addition is the required possibility using the correction circuit. BCD addition is same as binary addition when the result of the addition is same as binary addition when the result of the addition is beyond 9(1001), we must add 6(0110) to the original result. So two 4 bit parallel adders are used to get correct result. One of the adders is used to add the given BCD numbers. Second adder is first to determine the result of the previous one whether it exceeds the BCD range or not. If it is exceeding 0110 is added to the previous result. The result of the second adder is to generate the correct BCD output.

III. LITTERATURE SURVEY

Improving efficiency is achived by use of this logic.Moreover it will affect the speed of the circuits such as nano circuits and computing applications.[1] , Reversible logic circuits are constructed under two constrains(Fan-Out and loops/feedback) which are not permitted. It may be used along with other parameters such as constants, garbage, gate count, flexibility, quantum cost, gate levels which may optimize the circuit effectively.[2], The aim of this paper is to perform both BCD addition/subtraction is a single circuit. For this reason two new optimized gates are used which does not provide any restrictions. To operate this garbage output, gate count and constant input should be minimum.[3], The main focus of this paper is low power dissipation under 70nm technology by using RPS with BCD adder.[4], To obtain exact BCD value, the modified circuit which is the combination of parallel adder and overflow detection circuit is used.[5]

IV.PROPOSED ARCHITECTURE

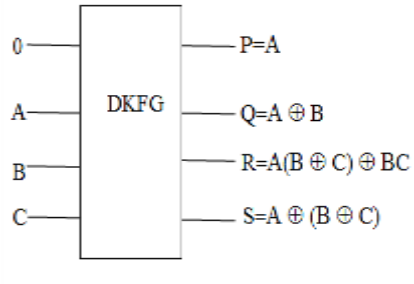


Fig DKFG GATE

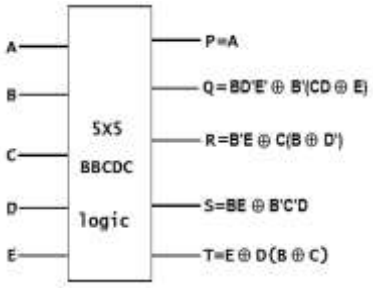


Fig BBCDC LOGIC

TABLE I TRUTH TABLE OF BBCDC

INPUTS					OUTPUTS				
E	D	C	B	A	T	S	R	Q	P
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	0	0	1	0
0	0	0	1	1	0	0	0	1	1
0	0	1	0	0	0	0	1	0	0
0	0	1	0	1	0	0	1	0	1
0	0	1	1	0	0	0	1	1	0
0	0	1	1	1	0	0	1	1	1
0	1	0	0	0	0	1	0	0	0
0	1	0	0	1	0	1	0	0	1
0	1	0	1	0	1	0	0	0	0
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	1	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1	0	0
0	1	1	1	1	1	0	1	0	1
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	1	0	1	1	1
1	0	0	1	0	1	1	0	0	0
1	0	0	1	1	1	1	0	0	1

Fig Table of BBCDC LOGIC

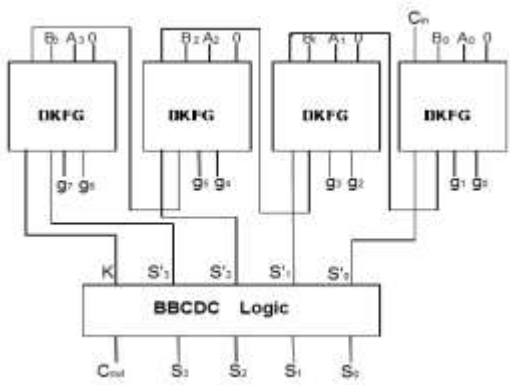


Fig BCD ADDER using Reversible Gates

V. RESULT

BCD ADDER USING BINARY ADDER AND

CORRECTION CIRCUIT

DIGIT	1	2	3	4	5
NUMBER OF SLICES	9	18	26	35	44
NUMBER OF LUTs	32	62	92	122	152
AREA	41	80	118	157	196
COMBINATIONAL DELAY(ns)	14.466	20.038	25.432	30.826	36.220
FREQUENCY(MHZ)	69.127	49.905	39.320	32.440	27.609
POWER(mw)	0.081	0.081	0.081	0.081	0.081

BCD ADDER USING NAND ONLY GATES

DIGIT	1	2	3	4	5
NUMBER OF SLICES	14	25	38	50	63
NUMBER OF LUTs	48	90	134	178	222
AREA	62	115	172	228	285
COMBINATIONAL DELAY(ns)	12.928	17.728	23.732	29.552	35.372
FREQUENCY(MHZ)	77.351	56.407	42.137	33.838	28.270
POWER(mw)	0.081	0.081	0.081	0.081	0.081

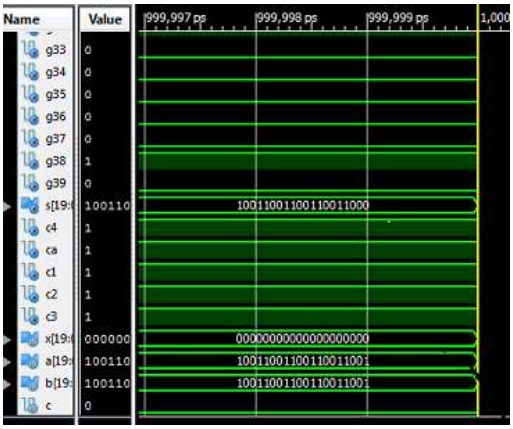
BCD ADDER USING REVERSIBLE LOGIC GATES

DIGIT	1	2	3	4	5
NUMBER OF SLICES	9	18	27	36	45
NUMBER OF LUTs	32	64	96	128	160
AREA	41	82	123	164	205
COMBINATIONAL DELAY(ns)	9.419	13.481	17.543	21.605	25.667
FREQUENCY(MHZ)	106.168	74.178	57.002	46.285	38.960
POWER(mw)	0.081	0.081	0.081	0.081	0.081

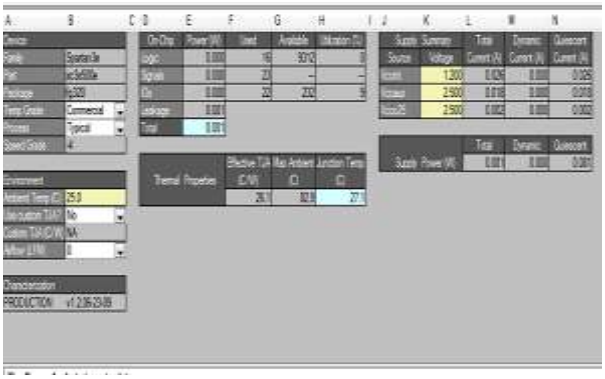
BCD ADDER DESIGN USING MULTIPLEXER

DIGIT	1	2	3	4	5
NUMBER OF SLICES	9	18	26	35	43
NUMBER OF LUTs	32	62	92	122	152
AREA	41	80	118	157	195
COMBINATIONAL DELAY(ns)	14.295	20.084	25.478	30.872	36.226
FREQUENCY(MHZ)	69.954	49.790	39.249	32.391	27.604
POWER(mw)	0.081	0.081	0.081	0.081	0.081

SIMULATION OUTPUT FOR BCD ADDER DESIGN USING REVERSIBLE GATES (5-DIGIT)

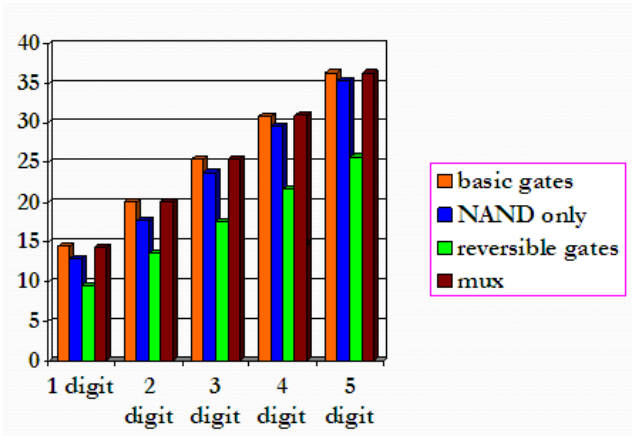


POWER OUTPUT (5-DIGIT)

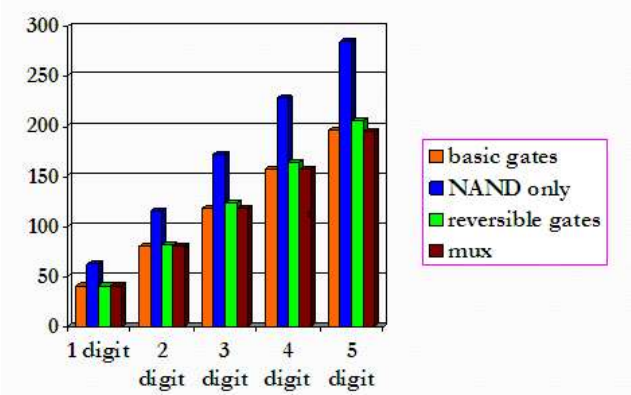


PICTOGRAPH

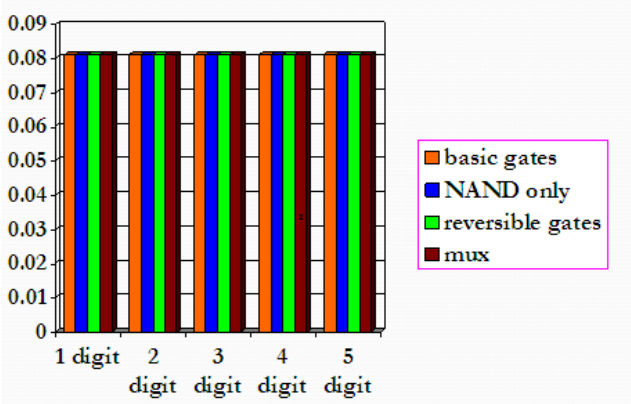
DELAY COMPARISON CHART



AREA COMPARISON CHART



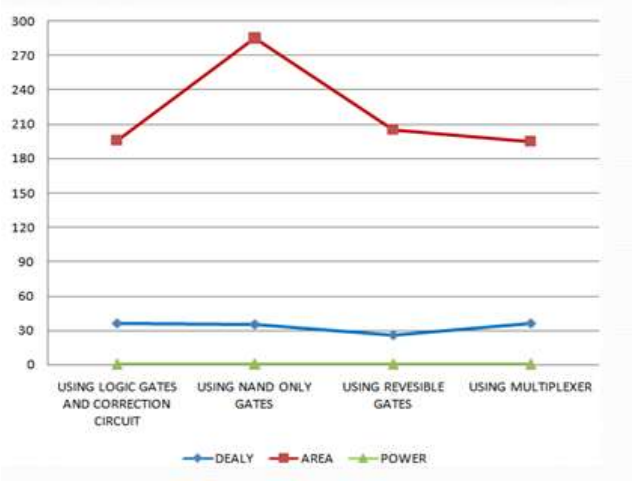
POWER COMPARISON CHART



COMPARISON TABLE FOR 5 DIGITS

ARCHITECTURE BCD ADDER DESIGN USING	DELAY(ns)	AREA	POWER(mw)
LOGIC GATES AND CORRECTION CIRCUIT	36.226	196	0.081
NAND ONLY GATES	35.372	285	0.081
REVERSIBLE GATES	25.667	205	0.081
MULTIPLEXER	36.226	195	0.081

PARAMETER COMPARISON CHART



VI.CONCLUSION AND DISCUSSION

In this project work we have designed four architectures of BCD ADDER for primarily optimizing the parameter like delay, area and power. These architectures Compute BCD addition up to 5 digits.

The optimization of delay in BCD ADDER using REVERSIBLE GATES is mainly considered to lesser delay. Even though various architectures are constructed in this project work, BCD ADDER using REVERSIBLE GATES gives 29% less delay compared to BCD

ADDER using BINARY ADDERS and CORRECTION CIRCUIT. Getting 27%delay reduction when compared to BCD ADDER using NAND ONLY gates and 29% delay is reduced compared with BCD ADDER using MULTIPLEXER.

Finally we concluded that lesser delay is achieved using BCD ADDER using REVERSIBLE GATES among all the above mentioned architectures.

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